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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/037,804 | 12/26/2001 | Toshihiro Yanagi | 49021-DIV (70904) | 6242 |

21874 7590 06/14/2004

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| EXAMINER | |
|---|---|
| OSORIO, RICARDO | |
| **ART UNIT** | **PAPER NUMBER** |
| 2673 | 10 |

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/037,804 | YANAGI ET AL. | |
| | Examiner | Art Unit | |
| | RICARDO L OSORIO | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *4,5,7,13-16,19 and 21-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,13-16 and 21-30* is/are allowed.

6)☒ Claim(s) *4,5,19,32 and 33* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 4-5, 19 and 32-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al (5,587,772).

Regarding claims 4, 19 and 32-33, Suzuki teaches of a display device comprising a plurality of pixel electrodes (col. 3, lines 30-31); image signal lines for supplying data signals to said pixel electrodes (col. 1, lines 14-18); a plurality of scanning signal lines provided so as to intersect said image signal lines (col. 1, lines 14-18); a driving circuit for outputting a scanning signal to actuate said scanning signal lines (it is inherently needed to have a scan line driving circuit), thin film transistors each having a gate, a source, and a drain which are connected with one scanning signal line, one image signal line, and one image electrodes, respectively, said thin film transistors being provided at the intersections of said image signal lines and said scanning signal lines, respectively (see col. 1, lines 14-22); wherein the scanning signal is composed of a gate-on voltage which causes said thin film transistor to attain an ON state and a gate-off voltage which

causes said thin film transistor to attain an OFF state (col. 3, lines 40-48); a shift register section composed of a plurality of flip-flops which are cascaded and to which a scanning timing control signal is supplied (col. 4, lines 54-58); slope control sections for controlling the slopes of the falls from the gate-on voltage to the gate-off voltage (col. 3, lines 25-48); and switch sections each of which switches the gate-on voltage for the gate-off voltage or vice versa according to an output of each flip-flop (col. 4, line 54-col. 5, line 10); wherein said driving circuit controls the slopes of the falls of the scanning signal based on gate voltage-drain currency characteristics, or the output impedance, of said thin film transistor so that the scanning signal falls at a predetermined slope (col. 3, lines 25-48 and col. 4, lines 26-39. It is inherent since the voltage-drain currency characteristics of the TFT naturally affect the slopes of the falls of the scan signal).

Regarding claim 5 Suzuki further teaches that the slope appears in the waveform in an area said thin film transistors are on (col. 4, lines 26-39).

Regarding claim 33, Suzuki teaches that the scanning signal falls forming the slope in the waveform part of the way from HIGH to LOW (col. 3, lines 40-50).

***Allowable Subject Matter***

2. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a statement of reasons for the indication of allowable subject matter: Claim 31 is allowable since certain key features of the claimed invention are not

taught or fairly suggested by the prior art. Specifically, in claim 31, based on the gate voltage-drain currency characteristics of said thin film transistors and so a change rate of the fall of the waveform in a vicinity of an input-side end of the scanning signal line is substantially equal to a change rate of the fall of the waveform in a vicinity of the other end of the scanning signal line. Because none of the prior art teaches or suggests this element, this feature, taken together with the other limitations of the claims, renders the claims allowable over the prior art.

4. Claims 7, 13-16 and 21-30 are allowable.

5. The following is an examiner's statement of reasons for allowance: Claims 21-30 are allowable since certain key features of the claimed invention are not taught or fairly suggested by the prior art. Specifically, in claims 21 and 25, based on one of the settings a change rate of the fall of the waveform in a vicinity of an input-side end of the scanning signal line so as to be substantially equal to a change rate of the fall of the waveform in a vicinity of the other end of the scanning signal line, a basis of signal delay transmission characteristics, a basis of a gate-voltage drain currency characteristic of pixel switching elements. Because none of the prior art teaches or suggests this element, this feature, taken together with the other limitations of the claims, renders the claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Arguments***

6. Applicant's arguments filed 4-8-2004 have been fully considered but they are not persuasive.

Applicant argues that Suzuki does not disclose, teach or suggest controlling the slopes of the falls of the scanning signal based on the gate voltage-drain currency characteristics of said thin film transistors.

Examiner disagrees because the voltage-drain currency characteristics of the TFTs naturally affect the slopes of the falls of the scan signals. It is always considered since the value of the resistance between the gate and the drain, based on the voltage received at the gate, will always have an effect on the control of the slopes of the falls of the scan signal.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ricardo L. Osorio whose telephone number is (703) 305-2248. The examiner can normally be reached on Mon-Thu from 7:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached at 305-4938.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231
**or faxed to: (703) 872-9314 (for Technology Center 2600 only)**
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Ricardo L. Osorio
Examiner
Art Unit: 2673

RLO
June 8, 2004

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600